We claim:

1. In a data switching system having a plurality of switching controllers for exchanging data units over a backplane, each controller having an interface for transmitting data on the backplane and an interface having a plurality of ports for receiving data off the backplane in parallel from all transmitting interfaces, wherein each port is assigned a different clock cycle within a repetitive timing cycle for initiating the release of a data unit to a queue, and wherein each data unit must pass a filtering check and a watermark check to receive queueing clearance, a method for conducting receive processing, comprising:

sequencing the data units for conducting a filtering check;

conducting the filtering check on the data units in accordance with the sequence;

conducting a watermark check on the data units;

filtering the data units which fail the filtering check;

delaying the data units which pass the filtering check and fail the watermark check, until the watermark check is passed; and

queueing the data units which pass the filtering check and the watermark check.

2. The receive processing method according to claim 1, wherein the step of sequencing the data units comprises:

(a) determining the ports on which the data units were received;

(b) determining the current clock cycle within a repetitive timing cycle;

(c) from the determinations in (a) and (b), assigning a priority to each data unit as a function of the number of clock cycles the data unit's port would have to

wait before initiating the release of the data unit in the event queueing clearance for the data unit were received; and

(d) sequencing the data units in accordance with their assigned priorities.

3. The receive processing method according to claim 2, wherein a data unit is assigned the lowest priority if the number of clock cycles the data unit's port would have to wait exceeds a threshold number, and wherein data units assigned the same priority are sequenced in accordance with their ports.

4. The receive processing method according to claim 1, wherein the step of conducting the watermark check comprises:

determining the size of the data unit for the current watermark check;

calculating a, where a is the sum of a minimum projected write address and the size of the current data unit;

calculating b, where b is the sum of a maximum projected write address and the size of the current data unit;

calculating c, where c is the sum of a watermark and the current read address;

determining if the data unit for the preceding watermark check received queueing clearance;

if the preceding data unit received queueing clearance and $b \leq c$, replacing the minimum projected write address with the maximum projected write address, passing the current data unit and replacing the maximum projected write address with b;

if the preceding data unit received queueing clearance $b > c$, replacing the minimum projected write address with the maximum projected write address and failing the current data unit;

if the preceding data unit did not receive queueing clearance and $a \leq c$, replacing the maximum projected write address with a and passing the current data unit; and

if the preceding data unit did not receive queueing clearance and $a > c$, failing the current data unit.

5. In a data queueing system including a plurality of ports each having a data unit for release to a queue and each assigned a different clock cycle within a repetitive timing cycle for initiating the release of the data unit to the queue, and wherein each data unit must pass a filtering check as a condition for receiving queueing clearance, a method for sequencing data units received on the ports for the filtering check, comprising:

(a) determining the port on which the data units were received;

(b) determining the current clock cycle within a repetitive timing cycle;

(c) from the determinations in (a) and (b), assigning a priority to each data unit as a function of the number of clock cycles the data unit's port would have to wait before initiating the release of the data unit in the event queueing clearance for the data unit were received; and

(d) sequencing the data units in accordance with their assigned priorities.

6. The sequencing method according to claim 5, wherein the data unit is assigned the lowest priority if the number of clock cycles the port would have to wait exceeds a threshold number and wherein data units assigned the same priority are sequenced in accordance with their ports.

7. The sequencing method according to claim 5, wherein the determination in (c) is made by consulting a pre-configured "look-up" table.

8. The sequencing method according to claim 5, wherein the filtering check is performed in a CAM integrated circuit.

9. In a data queueing system in which data units must pass a watermark check as a condition for receiving queueing clearance, a method for conducting the watermark check, comprising:

determining the size of the data unit for the current watermark check;

calculating a, where a is the sum of a minimum projected write address and the size of the current data unit;

calculating b, where b is the sum of a maximum projected write address and the size of the current data unit;

calculating c, where c is the sum of a watermark and the current read address;

determining if the data unit for the preceding watermark check received queueing clearance;

if the preceding data unit received queueing clearance and $b \leq c$, replacing the minimum projected write address with the maximum projected write address, passing the current data unit and replacing the maximum projected write address with b;

if the preceding data unit received queueing clearance $b > c$, replacing the minimum projected write address with the maximum projected write address and failing the current data unit;

if the preceding data unit did not receive queueing clearance and $a \leq c$, replacing the maximum projected write address with a and passing the current data unit; and

if the preceding data unit did not receive queueing clearance and $a > c$, failing the current data unit.

10. The method for conducting a watermark check according to claim 9, wherein the maximum projected write address and the minimum projected write address are initially configured to be zero.

11. The method for conducting a watermark check according to claim 9, wherein the watermark is a configurable constant.

12. The method for conducting a watermark check according to claim 9, wherein the read address is incremented in the amount of any dequeued data.

13. The method for conducting a watermark check according to claim 9, further comprising:

if the current data unit is failed and a stall mode is not active, activating the stall mode.

14. The method for conducting a watermark check according to claim 13, further comprising:

if the current data unit is passed and the stall mode is active, deactivating the stall mode.

15. In a data queueing system having a plurality of ports which include a first group and a second group, wherein each group has at least one port and no port within the first group is within the second group, a method of queueing and dequeueing data within a repetitive timing cycle, comprising:

for each port within the first group, on each of the clock cycles within the repetitive timing cycle on which the port has writing privileges, determining whether the port has data for release and, if the port has data for release, releasing data from the port to the queue, and otherwise reading data from the queue; and

for each port within the second group, on each of the clock cycles within the repetitive timing cycle on which the port has writing privileges, if the port has data for release, releasing data from the port to the queue.

16. The method of queueing and dequeueing data according to claim 15, further comprising:

assigning each port writing privileges on all but one clock cycle within the repetitive timing cycle.

17. The method of queueing and dequeueing data according to claim 15, wherein the number of ports within the first group is one.

18. The method of queueing and dequeueing data according to claim 15, wherein the queue has a number of "stacked" physical memories for receiving the released data which is less than the number of ports.

19. The method of queueing and dequeueing data according to claim 15, further comprising:

assigning each port a different clock cycle within the repetitive timing cycle for initiating the release of a new data unit, wherein each port may initiate the release of a new data unit only on its assigned clock cycle.

20. The method of queueing and dequeueing data according to claim 15, wherein data are released in constant-bit words, each word comprising a portion of a complete data unit.